Amiga

A1200_R1

Rev.1.38 (06.09.2012)

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	03/13/92	GRR	
1	Advance Engineering Release	06/29/92	GRR	
1a	Pilot Production Release	09/09/92	GRR	
1b	FTZ Production Release	09/09/92	GRR	
1d	FCC/FTZ Production Release	10/10/92	GRR	

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
R246	SMT	NTSC Color Burst	4
R202	SMT	PAL Color Burst	4
R625	SMT	Keyboard MPU Clock	9
R624	SMT	Keyboard/System Reset	9

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	5
CN2	DB9P	Mouse/Joystick 2	5
CN3	RCA-J	Right Audio Output	5
CN4	RCA-J	Left Audio Output	5
CN5	DB23S	External Floppy	8
CN6	DB25P	RS232 Serial Port	7
CN7	DB25S	Parallel Printer Port	7
CN8	SQ DIN	Power Supply Connector	13
CN9	DB23P	Video Output	6
CN10	RCA-J	Composite Video	4
CN11	DIL-34	Internal Floppy Signal	8
CN12	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Keyboard Status LED's	9
CN15	PCMCIA	PC"Memory Card"	11
P9	EDGE-80	Memory Bus Expansion	12

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCKQ	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCLOCK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive 0 (Floppy)	
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	**Pot Lines 1 X/Y (Joysticks)**	
POUT	Paper Out (Parallel Port)	
PPD[7:0]	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RI	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SIDE	Side Select (Floppy)	
STEP	Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
TXD	Transmit Data (RS232 Port)	
VMA	Valid Memory Address (68000)	
VPA	Valid Peripheral Address (68000)	
VSYNC	Vertical Sync (Video)	
WE	Write Enable (DRAM)	
WPROT	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
	** Credit Card and IDE Stuff? **	

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor 16MHz	2
U2	8374	Alice (AA Agnus)	2
U3	8364	Paula	5
U4	4203	Lisa (AA Denise)	4
U5	f023a	AA Gayle (CBM ASIC)	2,8,11
U6	asst	ROM 512Kx16, 150 nS	10
U7-8	8520	Amiga VIA, 1 MHz	7
U10-11	28F10	Flash Memory 128Kx8	10
U12	CXA1145	Sony Video Encoder	4
U13	68HC05	amiga Keyboard MPU	9
U49	PST518	Low Voltage Sense IC	9
U15	LF347	BiMOS Op-Amp	5
	TL084	BiCMOS Op-Amp	alt
U16-17	Asst	DRAM 256Kx16, 80nS	3
U18-19	Asst	DRAM 256Kx16 Optional	3
U20	391???	Budgie (ASIC)	2
U28	1488	EIA Line Driver	7
U29	1489	EIA Line Receiver	7
U30	BT101	Triple 8-bit Video DAC	4
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
Y451	XTAL	4.43619MHz PAL Burst	4
Y621	XTAL	3MHz Ceramic Resonator	9
X2	asst	PAL Video Modulator	4
	asst	NTSC Video Modulator	4

A1200 Rev 1->1d PCB

C.A.D. Generated
No manual changes may be made to this document

DIRECTORIES AND REVISION HISTORY

DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
LAST: GRR	09/09/92
CHKD:	
APPR:	

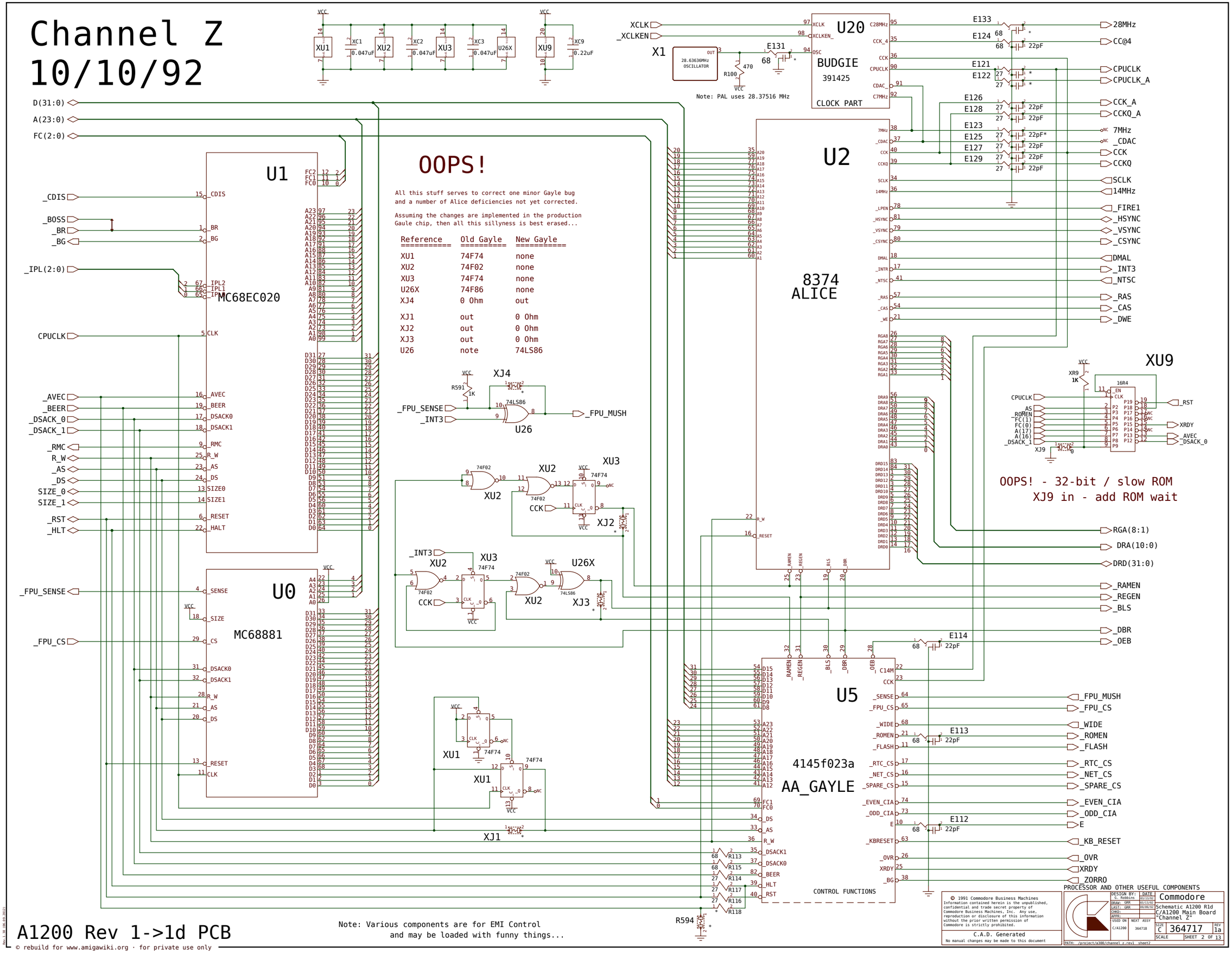
USED ON: C/A1200 | NEXT ASSY: 364718

Commodore
Schematic A1200 Rld
C/A1200 Main Board
"Channel Z"

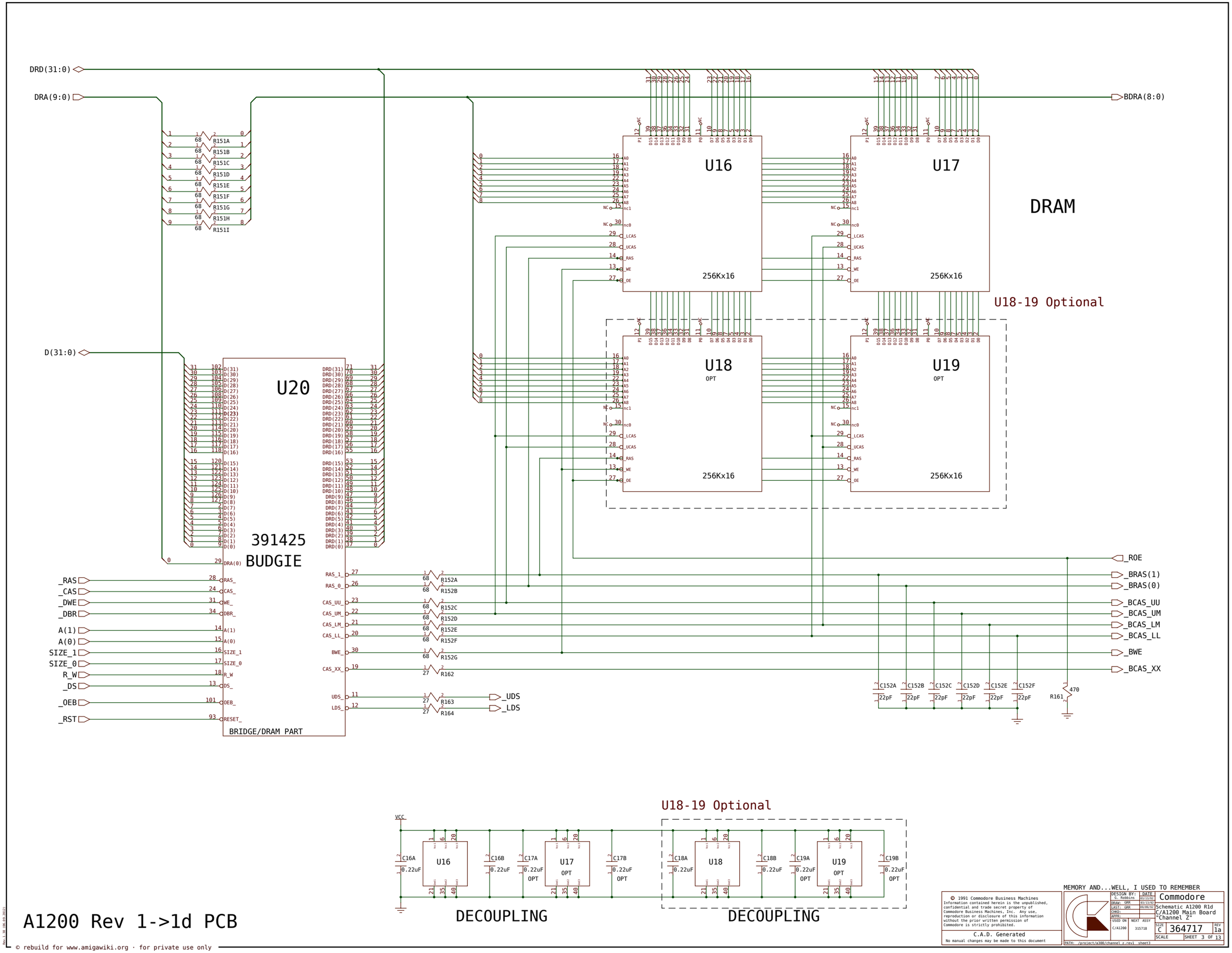
SIZE C | 364717 | REV 1a
SCALE | SHEET 1 OF 13

PATH: /project/a300/channel_z.rev1 sheet1

Channel Z
10/10/92



A1200 Rev 1->1d PCB



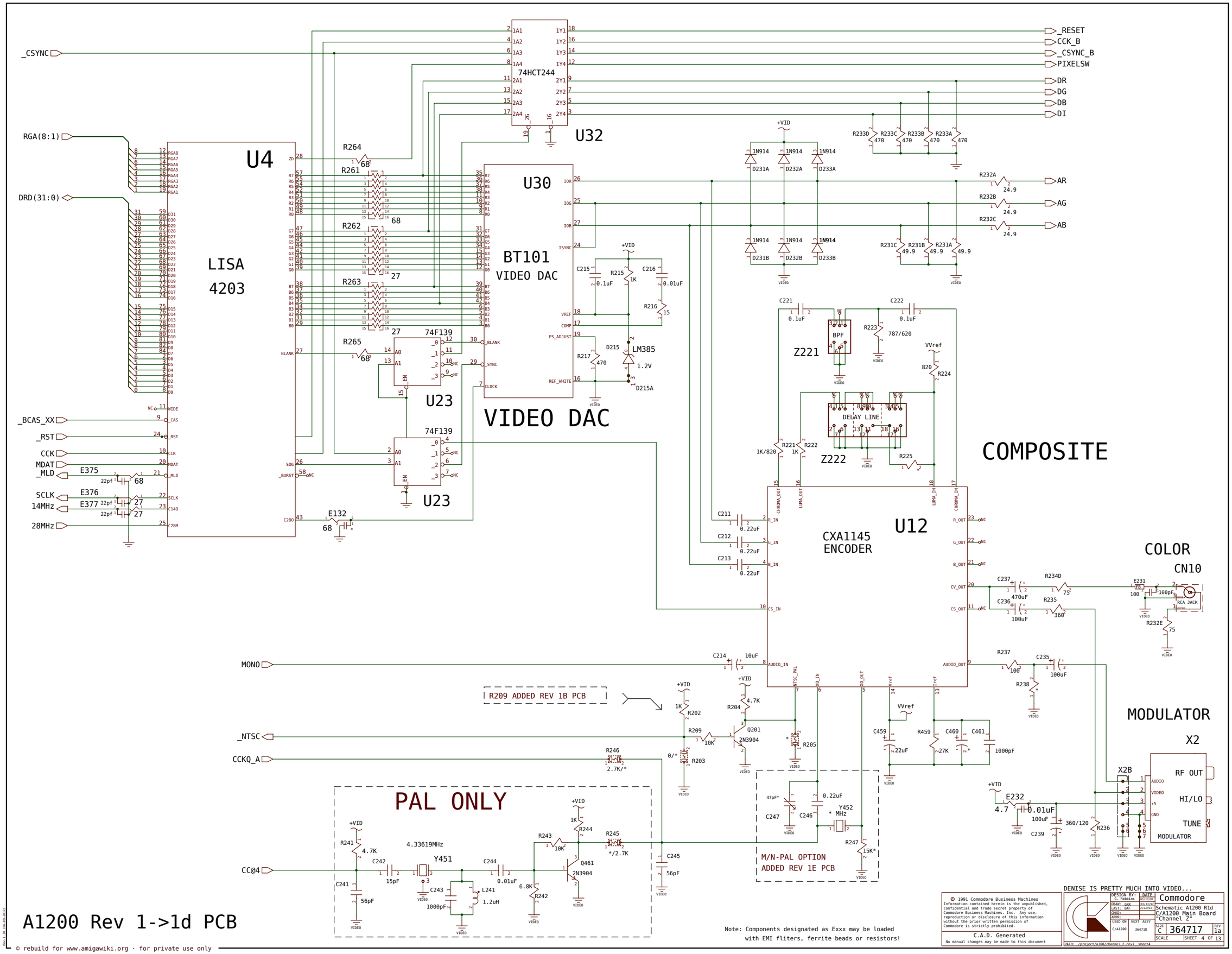
A1200 Rev 1->1d PCB

C.A.D. Generated
No manual changes may be made to this document

MEMORY AND...WELL, I USED TO REMEMBER

DESIGN BY: G. Robbins	DATE 01/11/92	Commodore
DRAW: GRR	01/11/92	Schematic A1200 R1d C/A1200 Main Board "Channel Z"
LAST: GRR	09/09/92	
CHKD:		
APPR:		
USED ON C/A1200	NEXT ASSY 315718	SIZE C 364717 REV 1a
		SCALE SHEET 3 OF 13

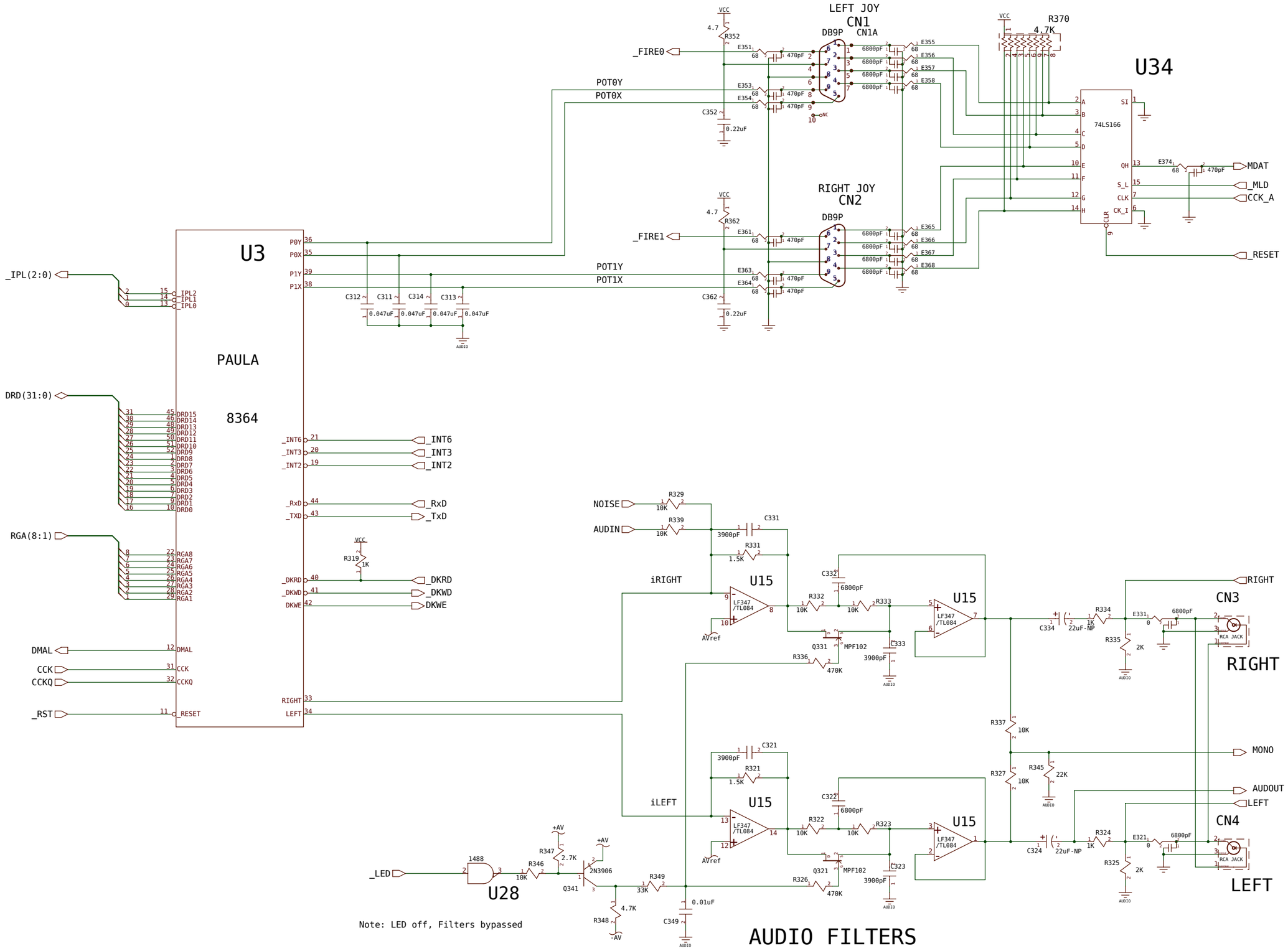
PATH: /project/a300/channel z.rev1 sheet3



Note: Components designated as Exxx may be loaded with EMI fliters, ferrite beads or resistors!

A1200 Rev 1->1d PCB

MOUSE/JOYSTICK PORTS



A1200 Rev 1->1d PCB

PAULA PREFERS THE TRADITIONAL MODES

C.A.D. Generated
No manual changes may be made to this document

		DATE
DESIGN BY:	G. Robbins	03/13/92
DRAW:	GRR	03/13/92
LAST:	GRR	09/09/92
CHKD:		
APPR:		
USED ON	NEXT	ASSY
C/A1200	364718	

Commodore

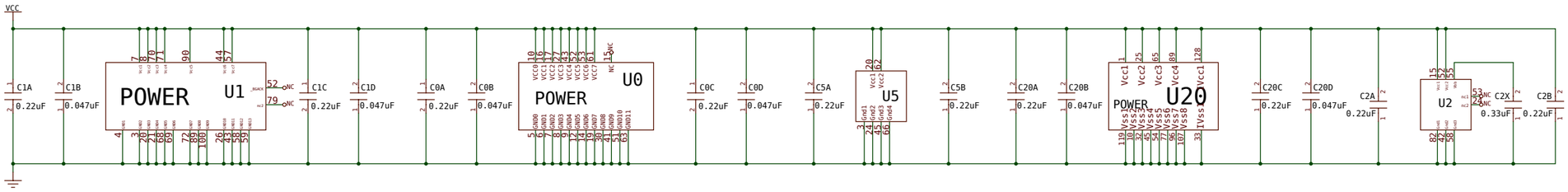
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"

SIZE C | 364717 | REV 1a

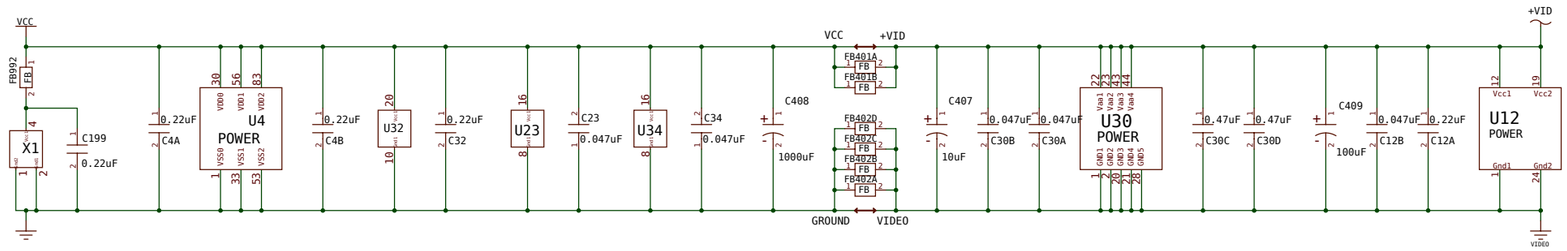
SCALE | SHEET 5 OF 13

PATH: /project/a300/channel_z.rev1 sheet5

GENERAL DECOUPLING



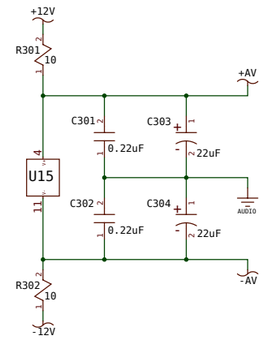
VIDEO DECOUPLING



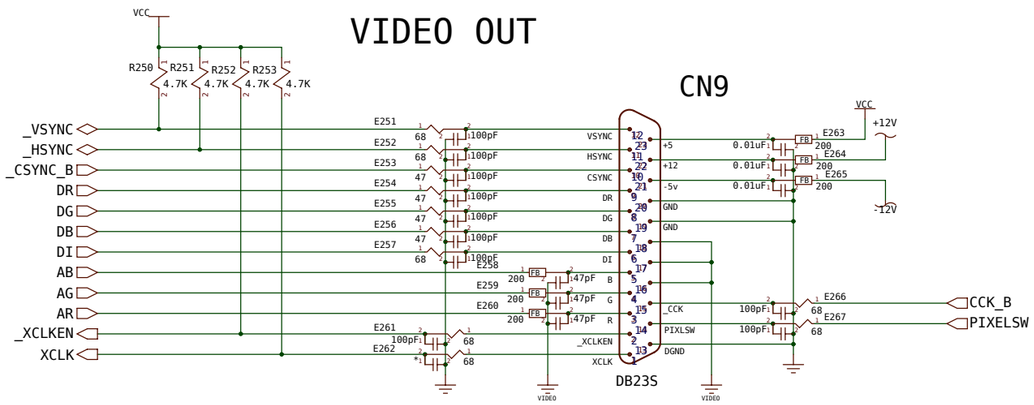
Note: As of Rev 1C, logic and video gound and power are
the same net, but reouted discretely except at DAC!

Also added C30C and C30D for overkill DAC decoupling.

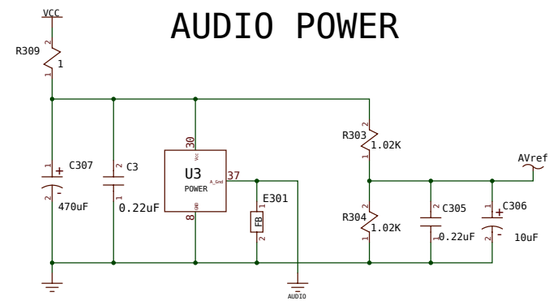
AUDIO DECOUPLING



VIDEO OUT



AUDIO POWER



Note: Ground interconnection near audio jacks.

A1200 Rev 1->1d PCB

PARTY OUT OF BOUNDS, WHAT A MESS...

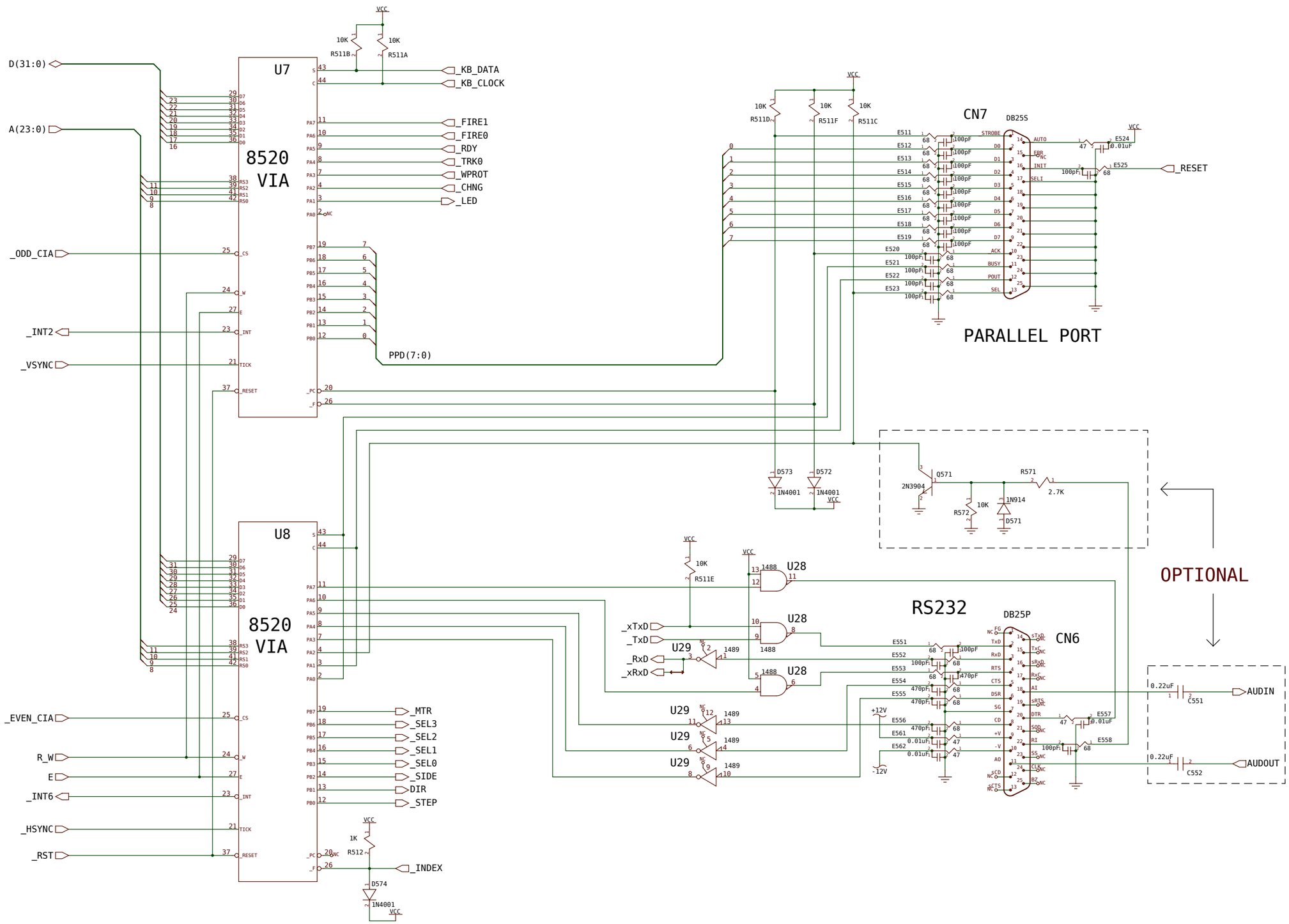
C.A.D. Generated
No manual changes may be made to this document

		DATE
DESIGN BY:	G. Robbins	03/13/92
DRAW:	GRR	03/13/92
LAST:	GRR	10/10/92
CHKD:		
APPR:		
USED ON	NEXT ASSY	
C/A1200	364718	

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"

SIZE C | 364717 | REV 1a
SCALE | SHEET 6 OF 13

PATH: /project/a300/channel_z.rev1 sheet6



SERIAL AND PARALLEL PORTS

C.A.D. Generated
No manual changes may be made to this document

	DESIGN BY:	DATE
	G. Robbins	03/13/92
DRAW:	GRR	03/13/92
LAST:	GRR	09/09/92
CHKD:		
APPR:		
USED ON	NEXT	ASSY
C/A1200	364718	

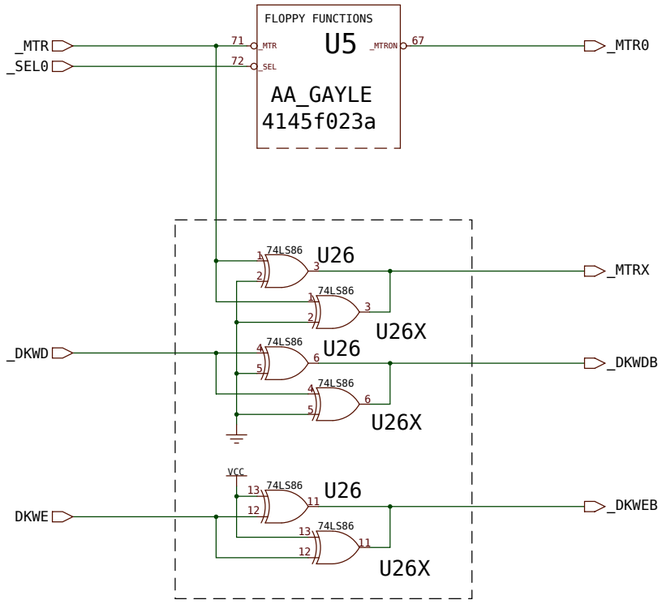
Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"

SIZE		REV
C	364717	1a
SCALE	SHEET 7 OF 13	

PATH: /project/a300/channel_z.rev1 sheet7

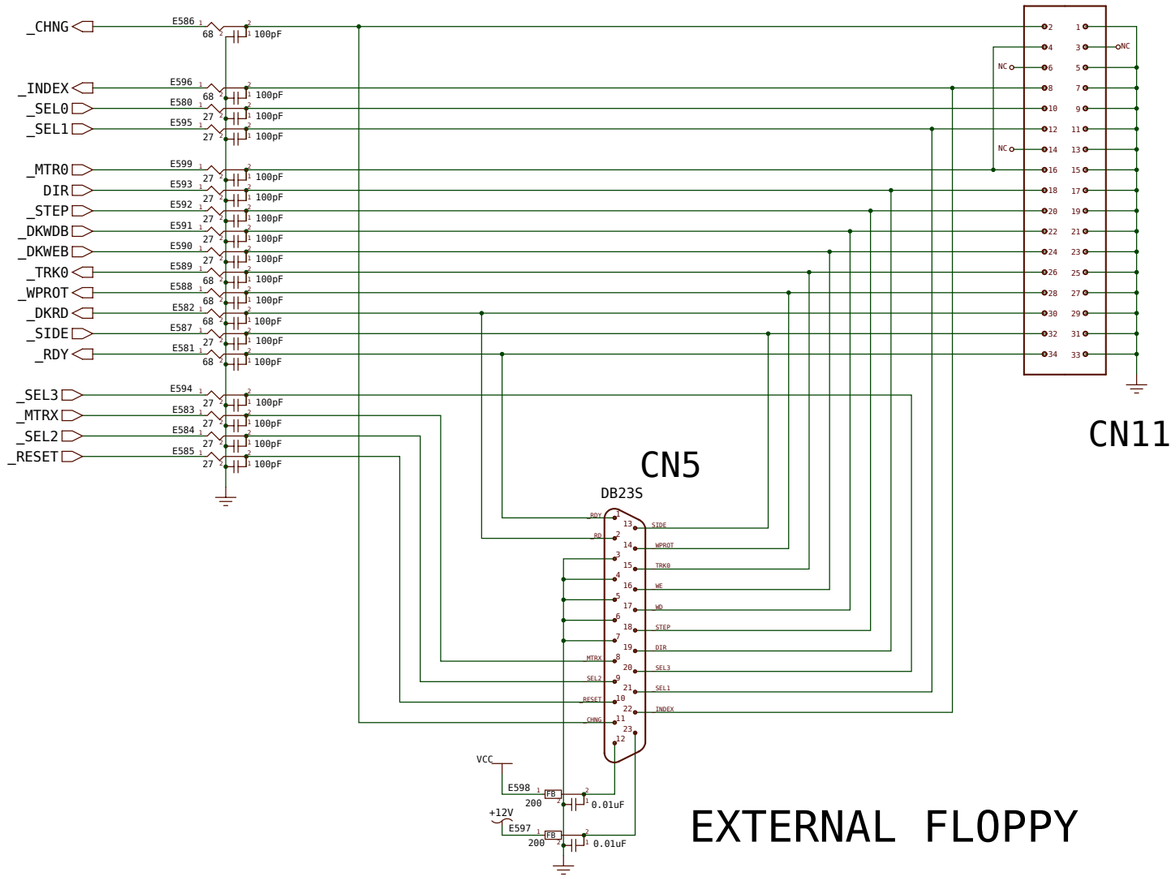
A1200 Rev 1->1d PCB

FLOPPY LOGIC



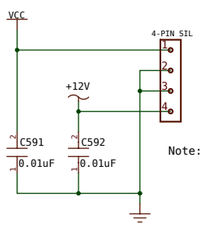
See OOPS on Page 2...
U26 and U26X may overlap!

INTERNAL FLOPPY



EXTERNAL FLOPPY

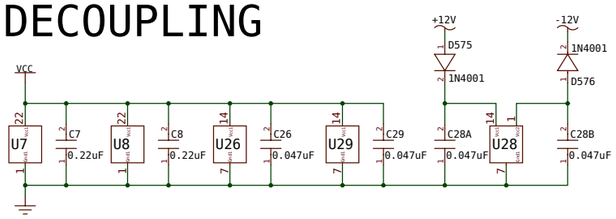
FLOPPY POWER



CN12

Note: Some drives are +5 only...

DECOUPLING



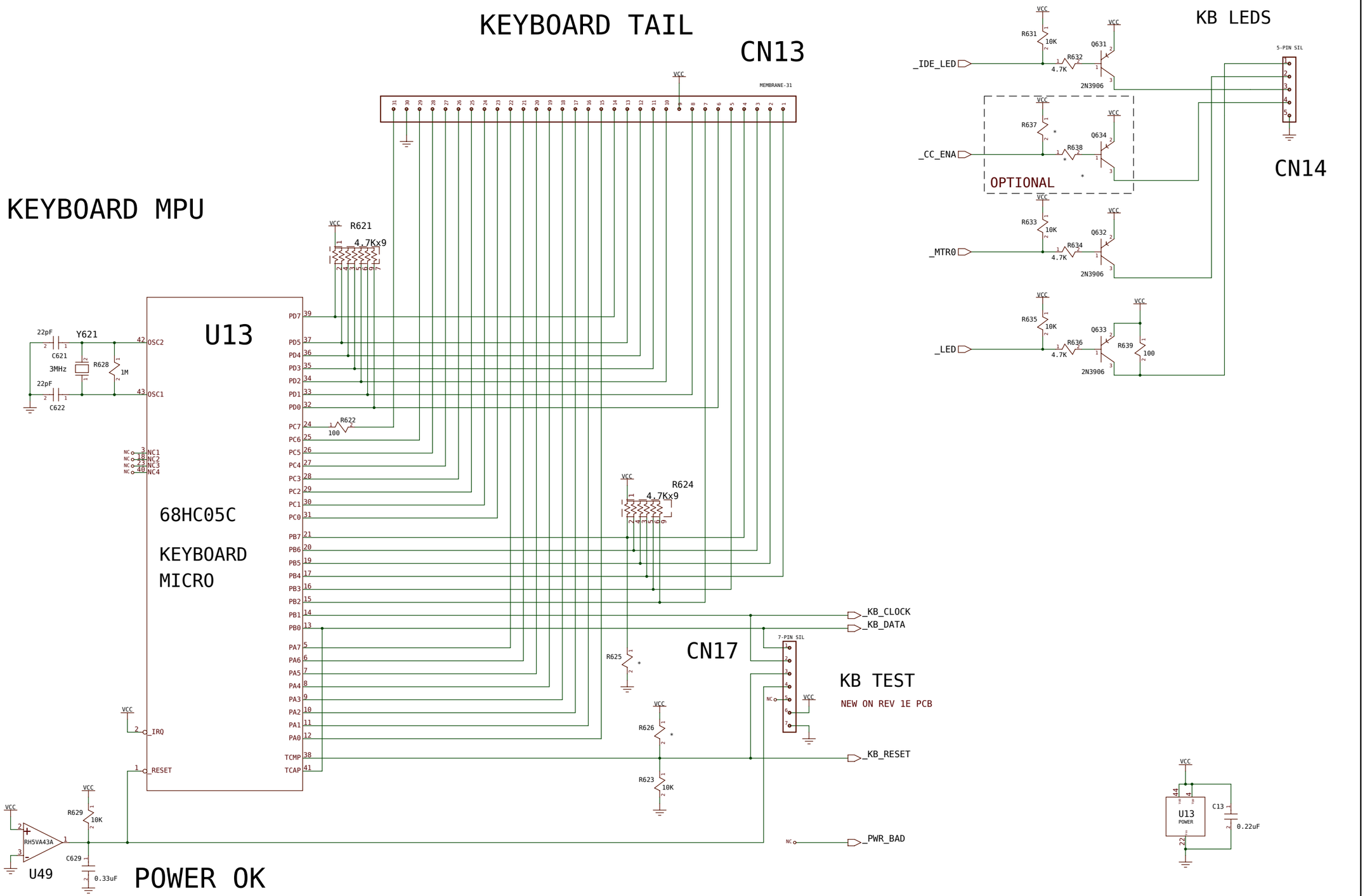
A1200 Rev 1->1d PCB

THE REST OF THE FLOPPY STUFF

C.A.D. Generated
No manual changes may be made to this document

DESIGN BY: G. Robbins	DATE 01/13/92	Commodore
DRAW: GRR	01/13/92	Schematic A1200 R1d
LAST: GRR	09/09/92	C/A1200 Main Board
CHKD:		"Channel Z"
APPR:		
USED ON C/A1200	NEXT ASSY 364718	SIZE C 364717 REV 1a
		SCALE SHEET 8 OF 13

PATH: /project/a300/channel z.rev1 sheet8



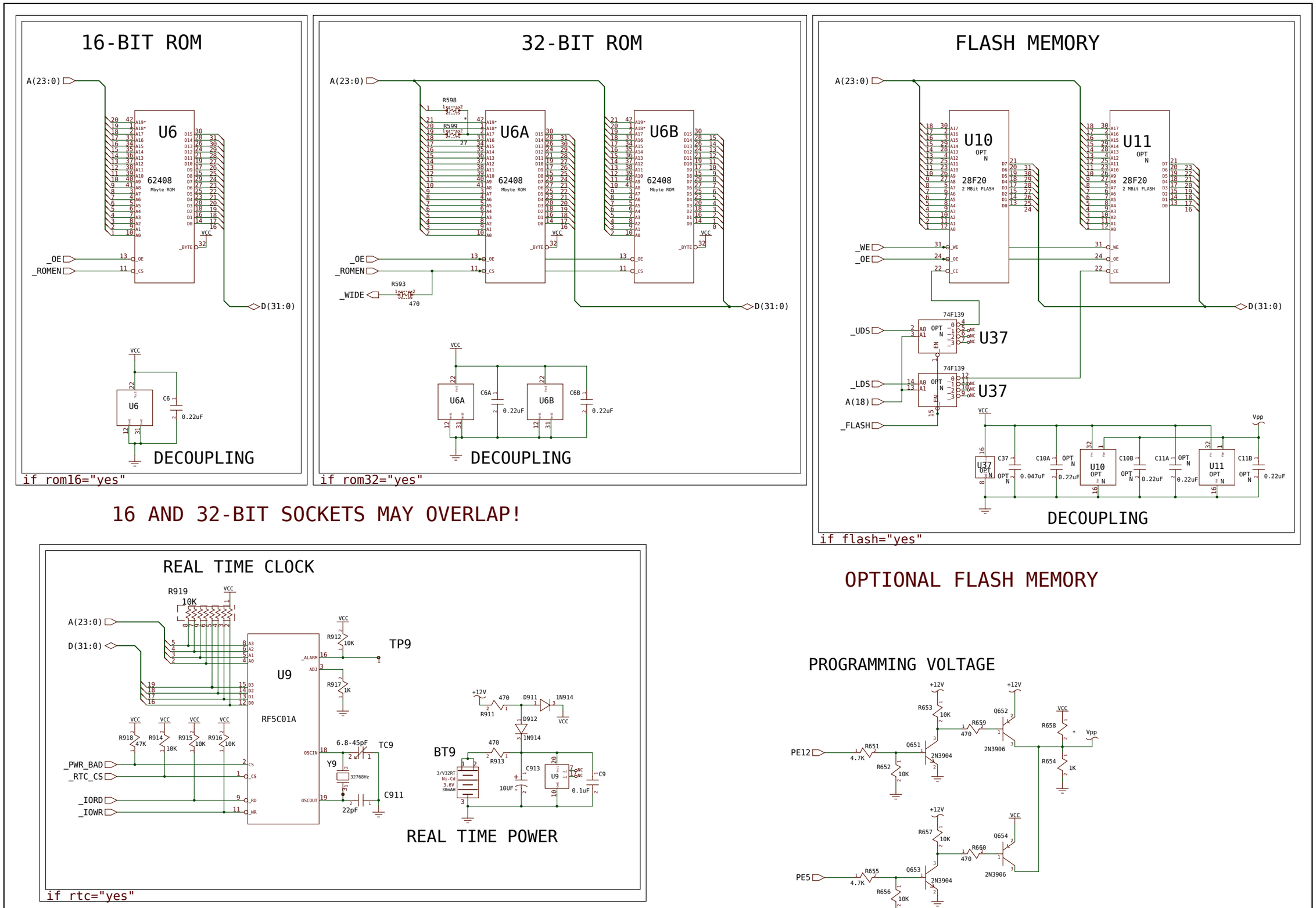
A1200 Rev 1->1d PCB

THE NEW HOME OF THE KEYBOARD VIRUS

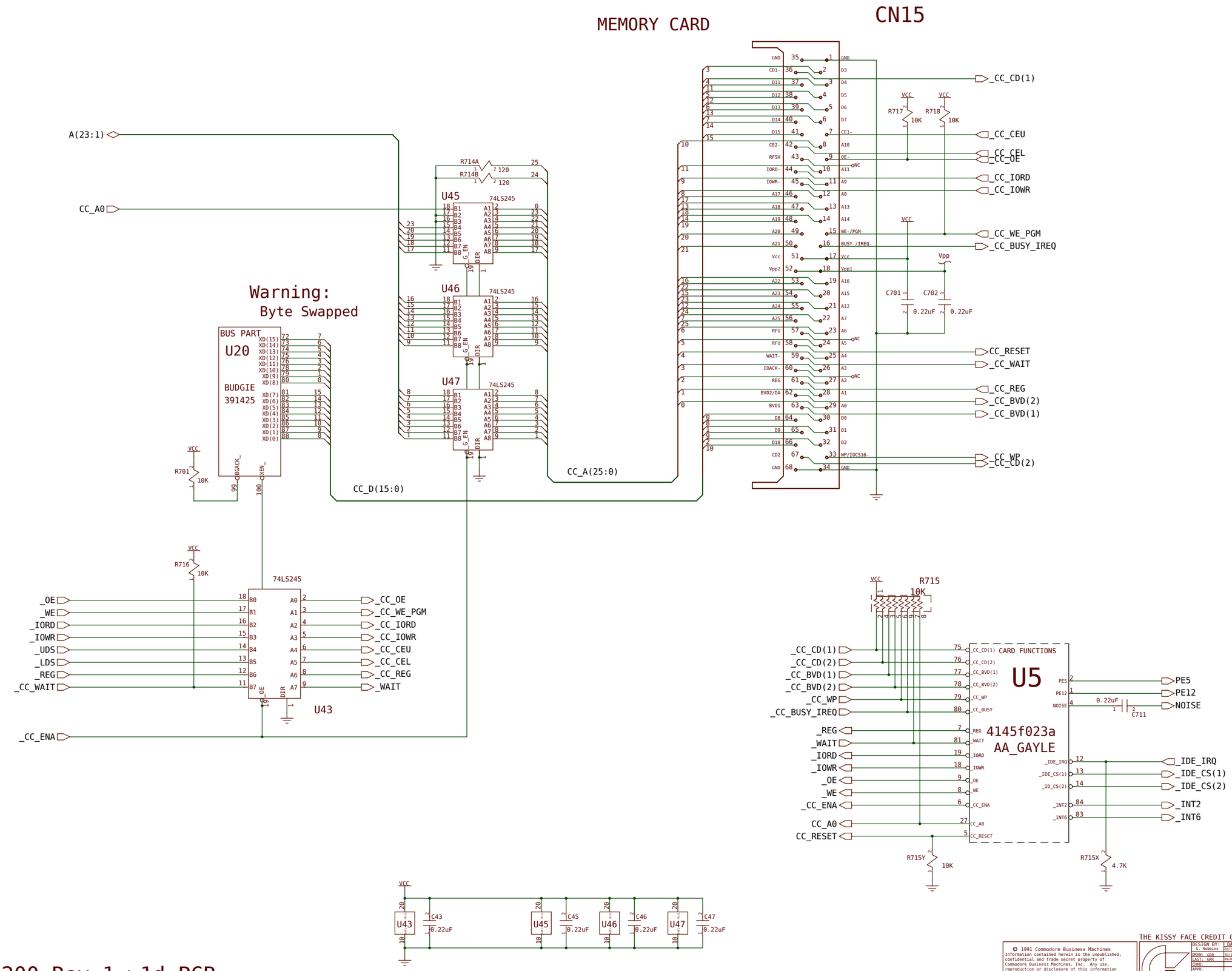
C.A.D. Generated
No manual changes may be made to this document

DESIGN BY: G. Robbins	DATE 01/13/92	Commodore
DRAW: GRR	01/13/92	Schematic A1200 R1d
LAST: GRR	09/09/92	C/A1200 Main Board
CHKD:		"Channel Z"
APPR:		
USED ON C/A1200	NEXT ASSY 364718	SIZE C 364717 REV 1a
		SCALE SHEET 9 OF 13

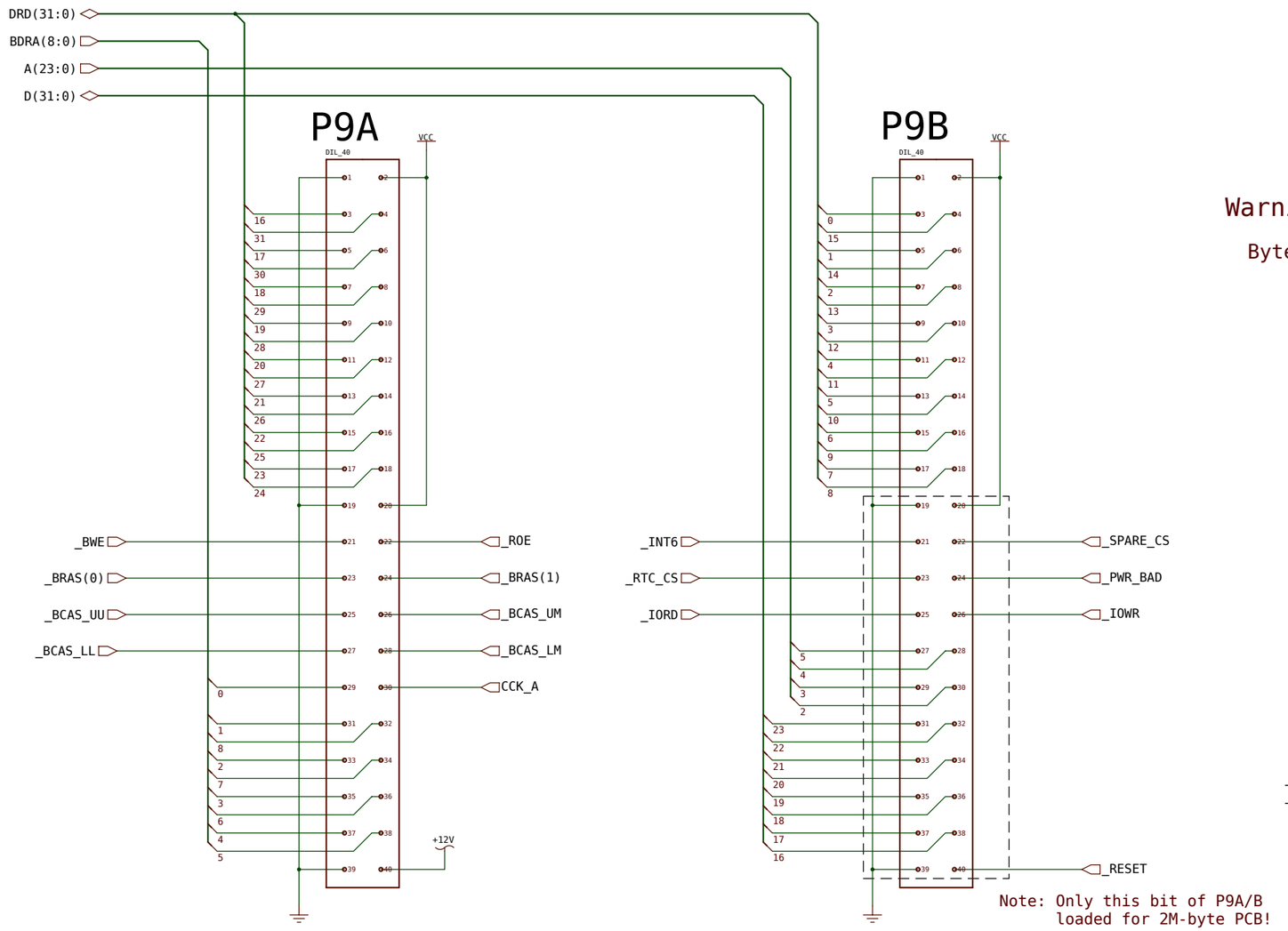
PATH: /project/a300/channel_z.rev1 sheet9



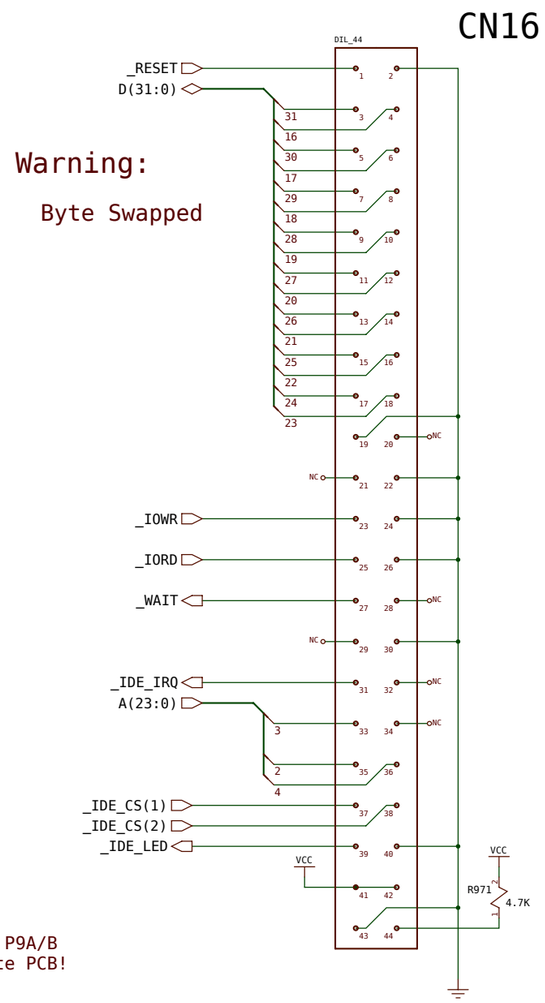
A1200 Rev 1->1d PCB



MEMORY EXPANSION



IDE DRIVE



A1200 Rev 1->1d PCB

C.A.D. Generated
No manual changes may be made to this document

MEMORY EXPANSION AND THE IDE DRIVE

DESIGN BY: G. Robbins	DATE 01/11/92
DRAW: GRR	01/11/92
LAST: GRR	99/99/92
CHKD:	
APPR:	
USED ON C/A1200	NEXT ASSY 364718

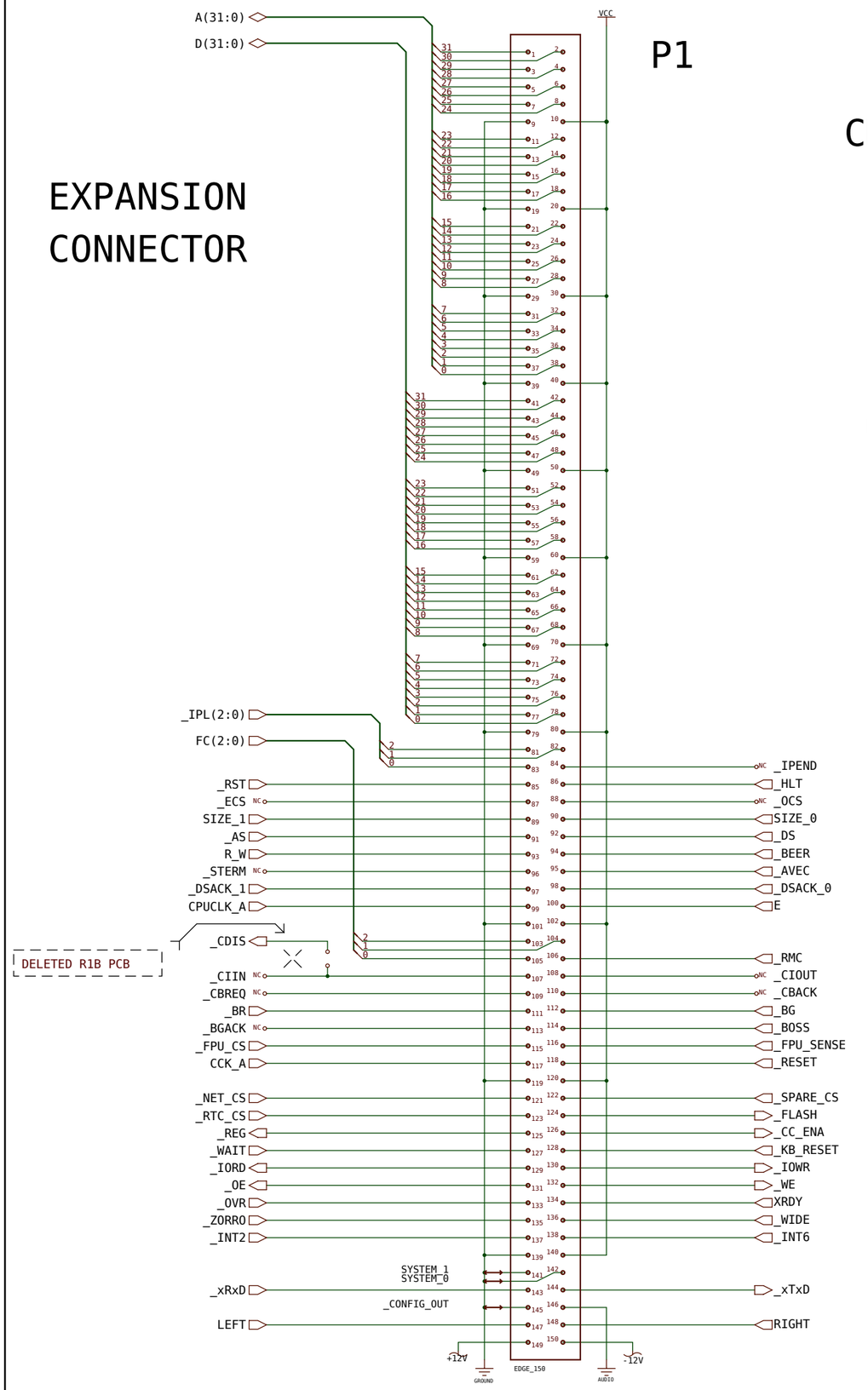
Commodore

Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"

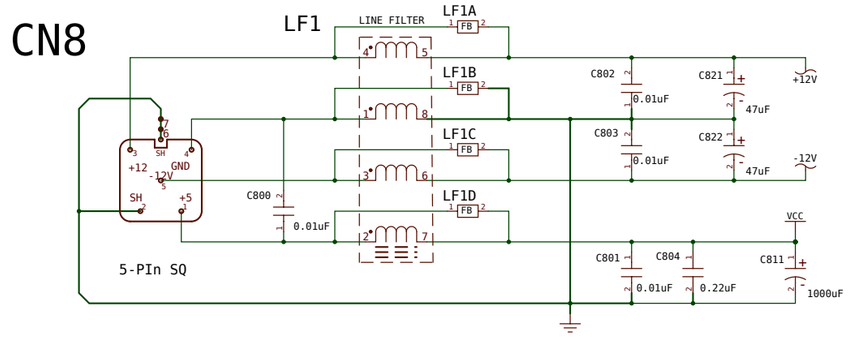
SIZE C | 364717 | REV 1a
SCALE | SHEET 12 OF 13

PATH: /project/a300/channel z/rev1 sheet12

EXPANSION CONNECTOR

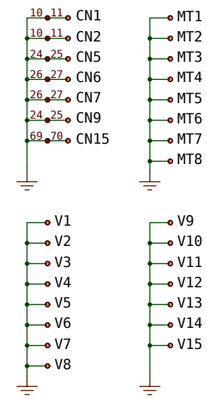


POWER INPUT

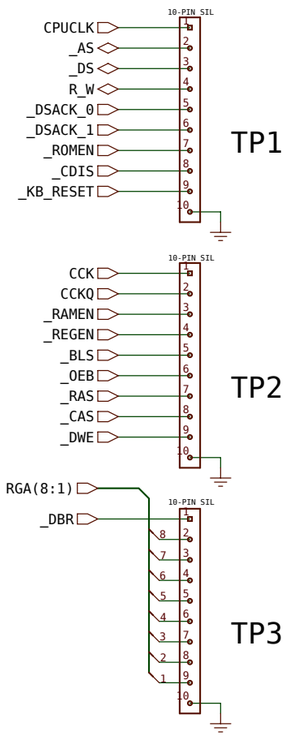


NOTE: HEAVY LINES INDICATE A
SINGLE POINT CONNECTION

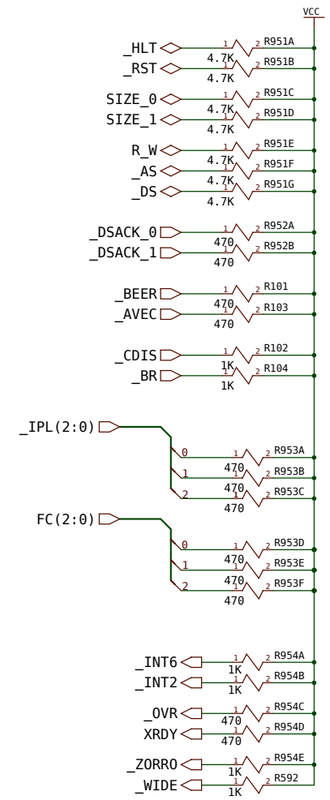
HOLES &c.



TEST ACCESS



TERMINATION



System Configuration Bits

SYSTEM	1	0	CPU/CPUCLK
	0	0	EC020/14MHz
	0	1	020/14MHz
	1	0	030/14MHz
	1	1	030/>14MHz

POWER DISTRIBUTION AND DECOUPLING

C.A.D. Generated
No manual changes may be made to this document

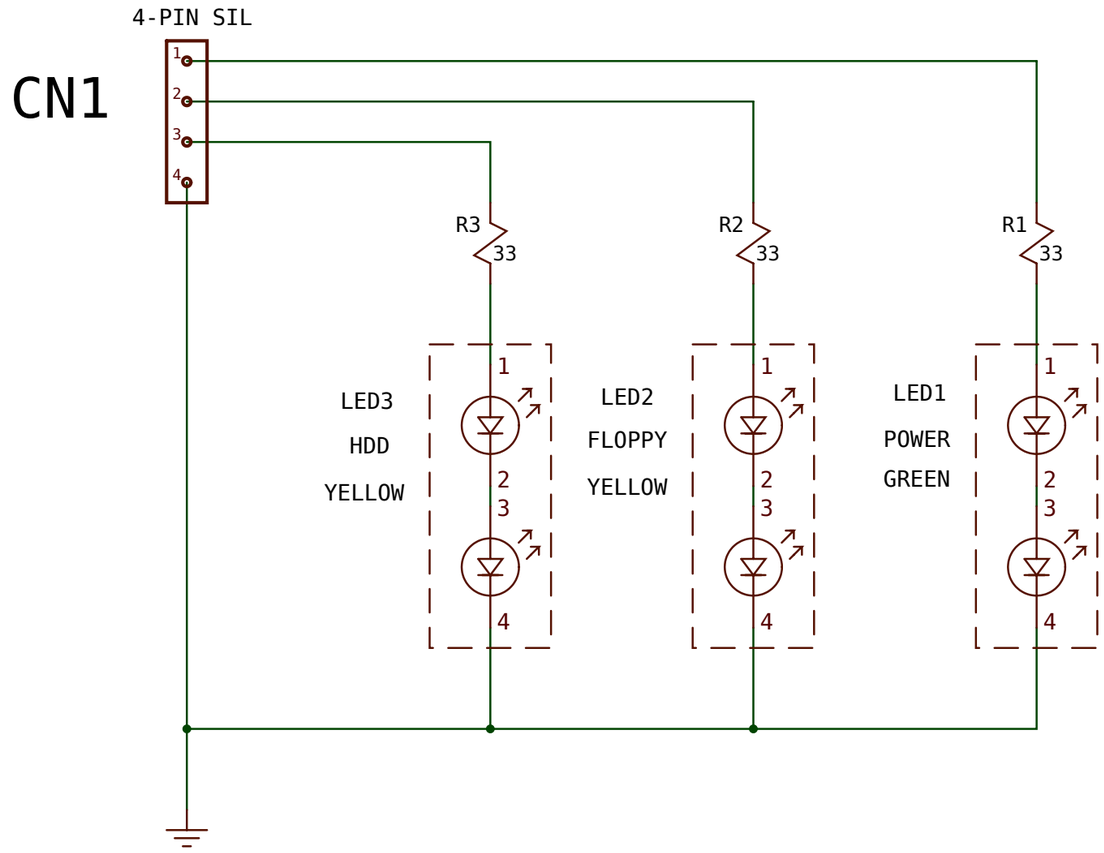
DESIGN BY: G. Robbins DATE 01/11/92
DRAW: GRR 01/11/92
LAST: GRR 10/10/92
CHKD:
APPR:
USED ON C/A1200 NEXT ASSY 364718

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
SIZE C 364717 REV 1a
SCALE
SHEET 13 OF 13
PATH: /project/a300/channel z/rev1 sheet13

A1200 Rev 1->1d PCB

Rev.1.38 (06.09.2012)

REVISIONS				
REV	DESCRIPTION	DATE	APRVL	MANAGER
1	ADVANCE ENGINEERING RELEASE			



SHINE ON, SHINE ON

A1200 LED PCB ASSEMBLY REV1

C.A.D. Generated
No manual changes may be made to this document

DESIGN BY:	DATE
B. FENIMORE	7/21/92
DRAW: BAF	7/21/92
LAST: BAF	7/21/92
CHKD:	
APPR:	

USED ON: A1200
NEXT ASSY: 364963

Commodore
SCHEMATIC
A1200 LED ASSY

SIZE A | 364966 | REV 1
SCALE | SHEET 1 OF 1

PATH: /user/fenimore/AA600/led_assy sheet1

Rev.1.38 (06.09.2012)